

Claims:

1. A format conversion circuit comprising:
 - a memory for storing video data;
 - header generation device for generating a packet header that adheres to a standard for motion picture compression;
 - synchronous timing detector for detecting a synchronizing signal for the video data; and
 - selection device for repeating the selection of the packet header generated by said header generation device and the selection of a predetermined amount of video data read out of said memory as a payload responsive to the packet header, during an interval from when said synchronous timing detection device detects the synchronizing signal until it detects the next synchronizing signal.
2. A format conversion circuit according to claim 1, wherein said selection device includes
 - a counter, reset in response to the synchronizing signal detected by said synchronous timing detector, for counting the amount of packet header output from said header generation device and the amount of video data read out of said memory, and
 - a switch, which selects the packet header generated by said header generation device until the amount of packet header counted by said counter reaches a predetermined amount, and selects the video data read out of said memory after the amount of packet header counted by said counter has reached the predetermined amount.
3. A format conversion circuit for converting the format of video data to a pseudo MPEG2-TS format, comprising:
 - a FIFO memory for storing the video data in response to a clock for the video data;

a header generation circuit for generating an MPEG2-TS packet header in response to the clock for the video data;

a synchronous timing detection circuit for detecting a horizontal synchronizing signal for the video data;

a counter, reset in response to the horizontal synchronizing signal detected by said synchronous timing detection circuit, for counting the number of bytes of packet header output from said header generation circuit and the number of bytes of video data read out of said FIFO memory; and

a switch, which selects the packet header generated by said header generation circuit until the number of bytes counted by said counter reaches the number of bytes of packet header as specified by MPEG2-TS, and selects the video data read out of said FIFO memory after the number of bytes counted by said counter has reached the number of bytes of packet header as specified by MPEG2-TS.

4. A format conversion circuit according to claim 3, wherein said counter outputs a data valid signal that indicates the validity of the data, the format of which has been converted to the pseudo MPEG2-TS format, while counting the number of bytes of packet header and the number of bytes of video data.

5. A format conversion circuit according to claim 4, wherein said FIFO memory is reset in response to the data valid signal output from said counter to erase the video data stored.

6. A method for converting the format of data, said method comprising:

storing video data;

generating a packet header that adheres to a standard for motion picture compression;

detecting a synchronization signal for the video

data; and

repeating the generation of a packet header and selecting a predetermined amount of the video data as a payload responsive to latter said packet header, during an interval between the detection of at least two of the synchronization signals.

7. A program storage device readable by a digital processing apparatus and having a program of instructions which are tangibly embodied on the storage device and which are executable by the processing apparatus to perform a method of converting the format of data, said method comprising:

storing video data;

generating a packet header that adheres to a standard for motion picture compression;

detecting a synchronization signals for the video data; and

repeating the generation of a packet header and selecting a predetermined amount of the video data as a payload responsive to latter said packet header, during an interval between the detection of at least two of the synchronization signals.